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NOAA Technical Memorandum ERL PMEL-9

VERSATILE RELEASE TIMER FOR FREE VEHICLE INSTRUMENTATION

Alex I. Nakamura
Robert R. Harvey

Pacific Marine Environmental Laboratory
Seattle, Washington
April 1977

noaa NATIONAL OCEANIC AND ATMOSPHERIC ADMINISTRATION / Environmental Research Laboratories

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A deep ocean, release timer unit was designed to provide a trigger for various explosive and nonexplosive release mechanisms. Complete details for construction, testing, and operation are provided.

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VERSATILE RELEASE TIMER FOR FREE VEHICLE INSTRUMENTATION

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Joint Tsunami Research Effort
Honolulu, Hawaii 96822

Pacific Marine Environmental Laboratory
Seattle, Washington
April 1977

UNITED STATES
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Laboratories
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CONTENTS

VERSATILE RELEASE TIMER FOR FREE VEHICLE INSTRUMENTATION[1]

Alex I. Nakamura and Robert R. Harvey[2]

Joint Tsunami Research Effort
Pacific Marine Environmental Laboratory
Environmental Research Laboratories, NOAA

A deep ocean, release timer unit was designed to provide a trigger for various explosive and nonexplosive release mechanisms. Complete details for construction, testing, and operation are provided.

1. INTRODUCTION

Recent oceanographic instrument development has moved largely in the direction of untethered packages known variously as free vehicle, pop-up, autonomous or free drop systems. Release of an expendable anchor is typically effected by either an acoustic recall or a preset timer device. We will discuss an economical release timer which is intended to activate a wide variety of release mechanisms.

Traditional instrument design often incorporates release electronics into the recording package. Although this somewhat simplifies the design, due to the common power supply and pressure housing, it limits the reliability and versatility since the release system is dependent on the integrity of the main pressure vessel. Also, release electronics become susceptible to interference from nearby circuitry and the built-in nature makes changes such as multiple release options difficult to implement. Our intention was to construct a totally independent, low-cost timer which could activate release devices whose active elements include explosive bolts (Sessions, 1973; Hill, 1974), explosive guillotines (Olsen, 1973), squibs (Sokolowski and Miller, 1968), wire corroding devices (Boegeman and Pavlicek, 1974), wax melting devices (Suckling, 1975), and solenoids (Morrison and Sternberg, 1973). The release package consists of (1) pressure case and electronics housing, (2) electronic timer, (3) release mechanism, and (4) release test set.

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[1]HAWAII INSTITUTE OF GEOPHYSICS CONTRIBUTION NO. 825.

[2]HAWAII INSTITUTE OF GEOPHYSICS, UNIVERSITY OF HAWAII, HONOLULU, HAWAII 96822.

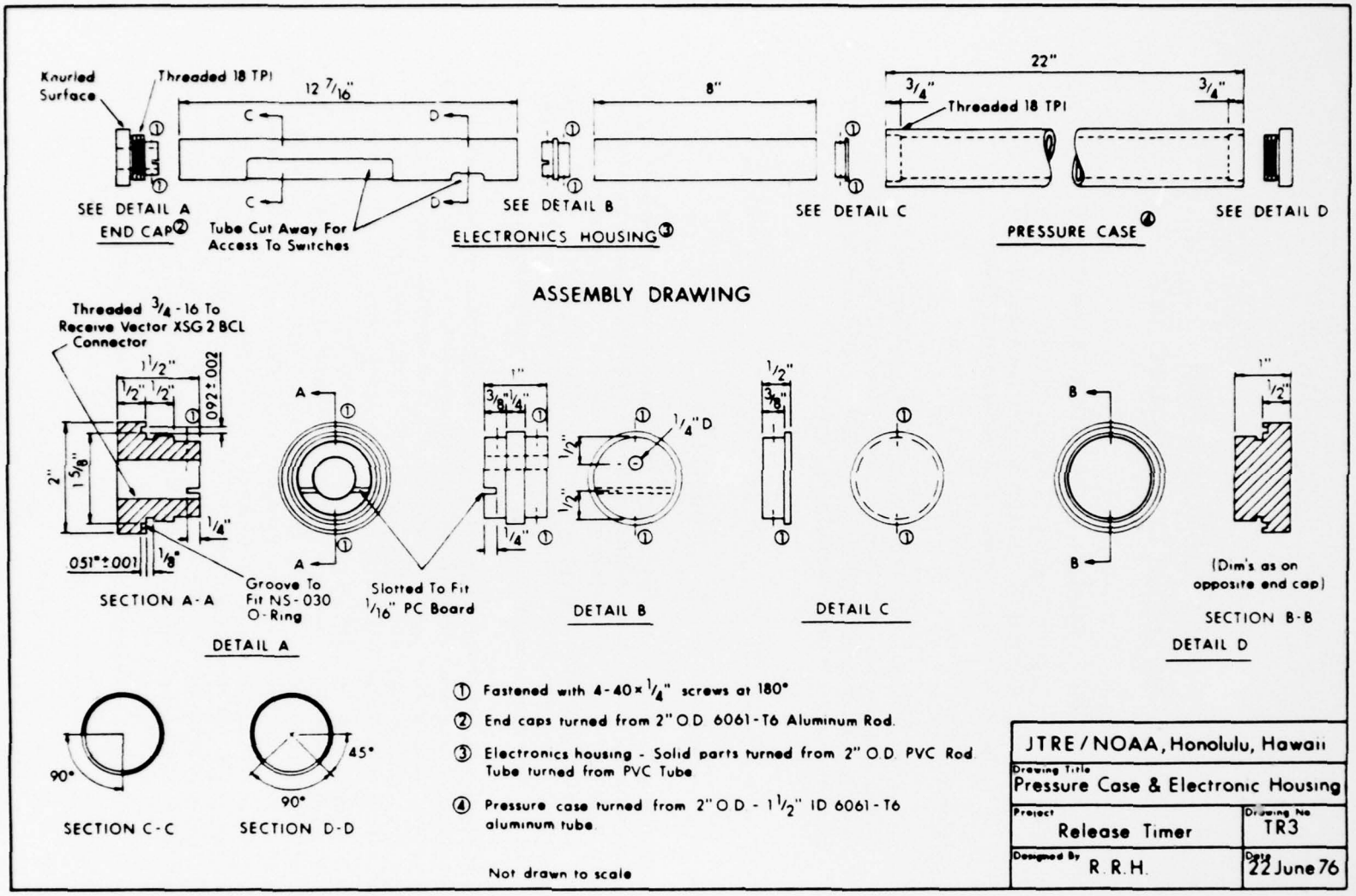


Figure 1. Mechanical drawing of release timer pressure case and electronics housing.

2. PRESSURE CASE AND ELECTRONICS HOUSING

The pressure case, including end caps, is fabricated from 6061-T6 aluminum (Fig. 1). The design depth is 7000 m; all pressure cases are tested to 12,000 psi, equivalent to 8500 m water depth, before installing electronics. The polyvinyl chloride (PVC) electronics housing protects and insulates the circuitry from the case; a second PVC tube supports the batteries.

The battery pack is assembled by soldering No. 18 stranded wire directly to the terminals of three "D" size alkaline cells so that they are connected in series. They are then mounted in line in the PVC tube. The lead wires enter the electronics housing through a 0.25 inch hole in the bulkhead separating the batteries and electronics. The printed circuit board is held prisoner in two grooves at either end of the housing.

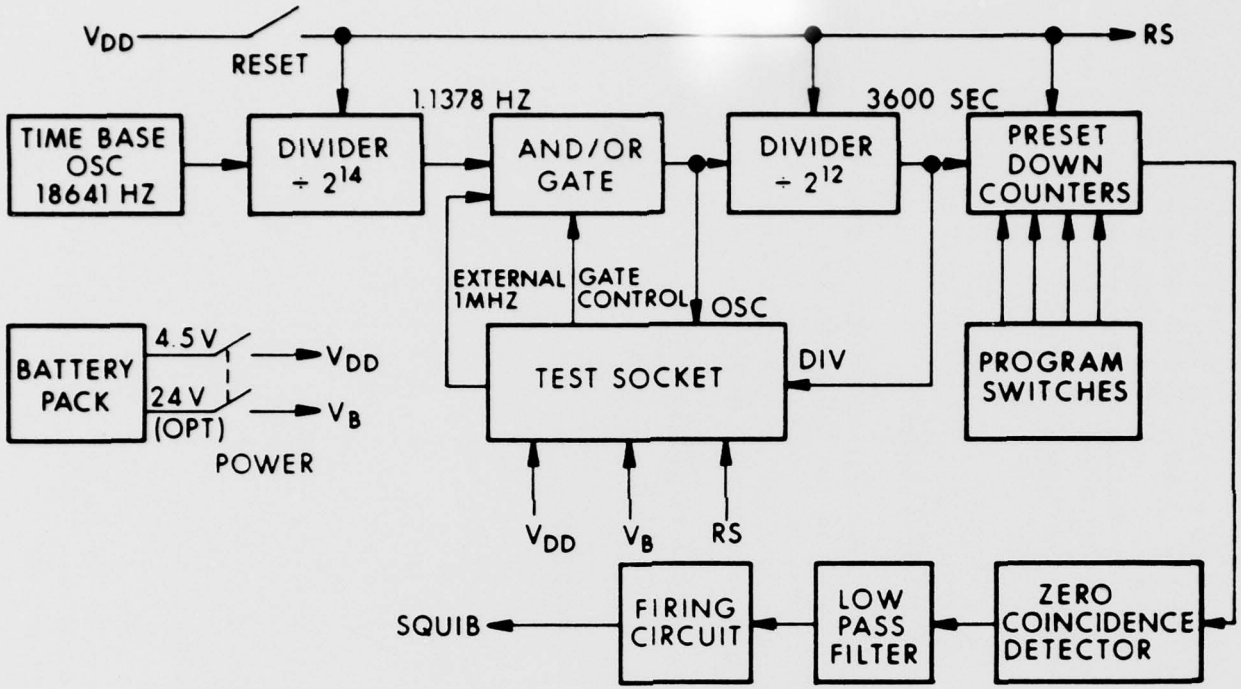
3. ELECTRONIC TIMER

The block diagram of the release timer electronic circuitry is shown in Figure 2; circuit details appear in the schematic diagram (Fig. 3). Complementary Metal Oxide Semiconductor (CMOS) integrated circuits are used throughout because of their inherent low power dissipation, high noise immunity, and noncritical power supply requirements.

The release timer circuitry can be divided into nine functional parts:

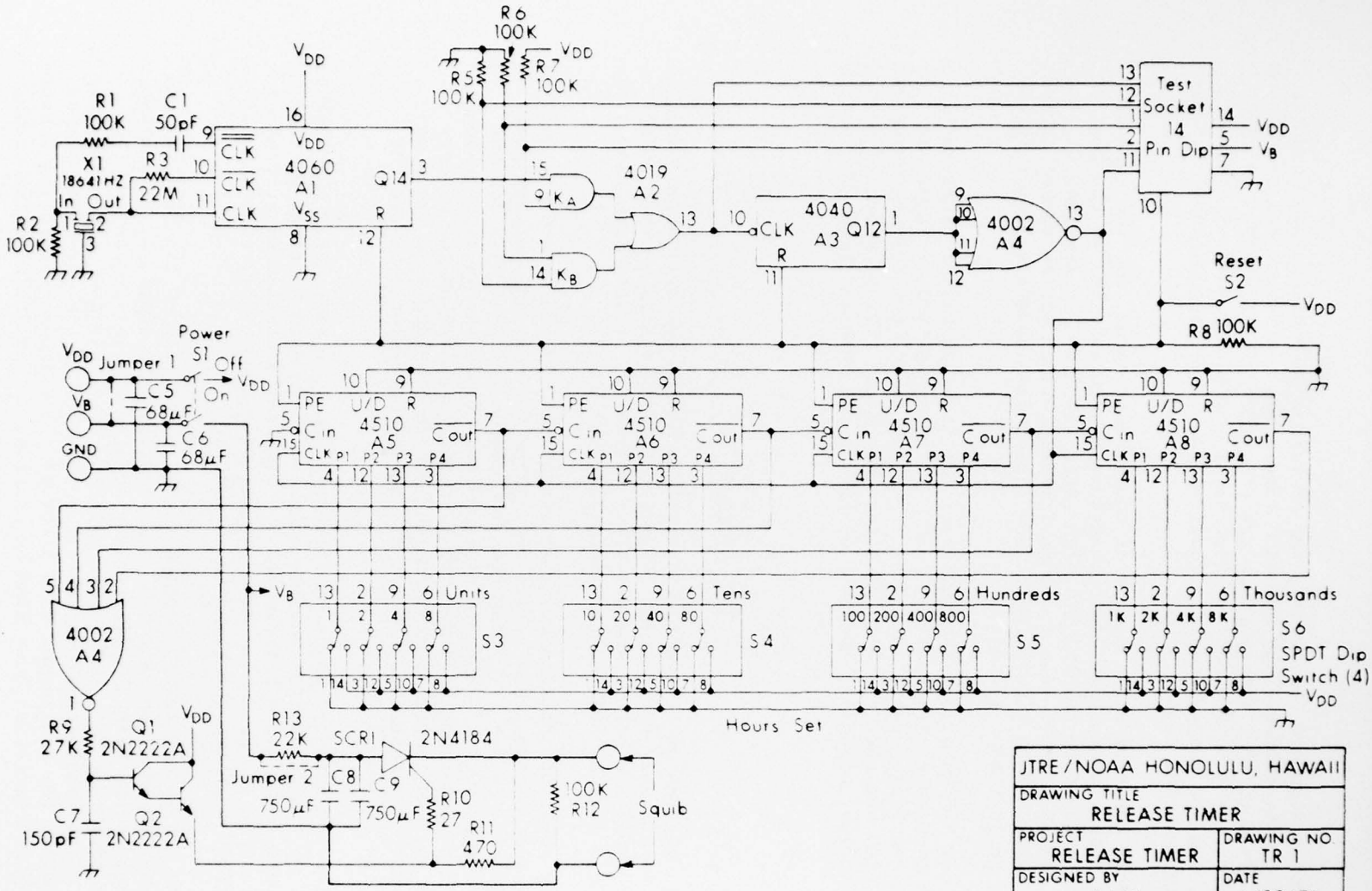
1. time base oscillator
2. first and second binary dividers
3. AND/OR select gate
4. preset down counters
5. time interval programming switches
6. zero coincidence detector
7. low-pass filter
8. squib firing circuit
9. battery pack

The time base oscillator consists of a low frequency quartz crystal with amplifiers (in A1) to sustain oscillation. The first binary divider, A1, divides the primary 18641 Hz signal down to 1.1378 Hz. The AND/OR gate then selects either this time base generated signal or an external test signal to feed the second binary divider, A3. The output from A3 is one pulse per 3600 s, or 1 hr, when the input is 1.1378 Hz. Crystal specifications indicate a frequency variation of +0.0065% to -0.025% over the temperature range 0° to 70° C, which greatly exceeds the conditions experienced in deep ocean use. This variation produces a maximum timing error of about 20 sec per day.



JTRE / NOAA HONOLULU, HAWAII	
DRAWING TITLE BLOCK DIAGRAM, RELEASE TIMER	
PROJECT TEST SET, RELEASE TIMER	DRAWING NO. TR 8
DESIGNED BY AIN	DATE 2-23-77

Figure 2. Block diagram of release timer.



JTRE/NOAA HONOLULU, HAWAII	
DRAWING TITLE: RELEASE TIMER	
PROJECT: RELEASE TIMER	DRAWING NO.: TR 1
DESIGNED BY: AIN	DATE: 6/22/76

Figure 2. Circuit diagram of release timer.

Preset counters A5, A6, A7, and A8 form a four decade down counter whose contents decrement by one each time a pulse arrives from the second binary divider, A3. The counters are programmed for the required time interval (from 1 to 9999 hr) by four binary coded decimal switches S3, S4, S5, and S6. Depressing the reset switch loads the contents of these switches into the counters.

After the programmed number of hours has elapsed, all the counters contain zeros, causing the zero coincidence detector, A4, to change from a low to high state, applying a high logic level to the low-pass filter comprising R9 and C7. The low-pass filter prevents narrow spikes caused by the nonsynchronous counting of the preset down counters from triggering the squib firing circuit.

After a 3 μs delay, the output of the low-pass filter rises sufficiently to turn on transistors Q1 and Q2 which, in turn, trigger the silicon controlled rectifier, SCR1. SCR1 activates the release mechanism either with the energy stored in capacitors C8 and C9, or directly from the batteries, depending upon the option chosen when the timer was assembled.

3.1 OPTIONS

Two methods of activating the release device are available. One option is suitable for release devices requiring a high current pulse such as explosive bolts, and the other option for devices requiring a continuous current such as wire corroding devices.

The pulse option requires that components R13, C8, and C9 be installed and jumpers 1 and 2 left out. Thus two separate battery packs are required: 4.5 V (V_{DD}) for the electronics and 24 V (V_B) for the squib firing circuit. The filter capacitor C6 and energy storage capacitors C8 and C9 must have working voltages greater than the battery voltage V_B, and they must also be low leakage and long life types to insure that the batteries are not discharged excessively before the release is activated.

The 24-V battery can be a mercuric-oxide type since only the leakage current of the capacitors need be supplied to sustain a charge on the capacitors. The 4.5 V battery for V_{DD} supplies a continuous current of approximately 100 μA to the electronics. A 1-ampere-hour capacity battery safely operates the timer for 6 months.

The continuous current option requires that components R13, C8, and C9 be omitted and jumpers 1 and 2 be installed. A single 4.5-V battery pack then powers both the electronics and the release mechanism. The battery pack must have sufficient capacity to supply 100 μA continuously to the timer, while retaining sufficient energy to activate the release device after the programmed time interval. The ambient operating temperature of the batteries must also be considered in calculating the required

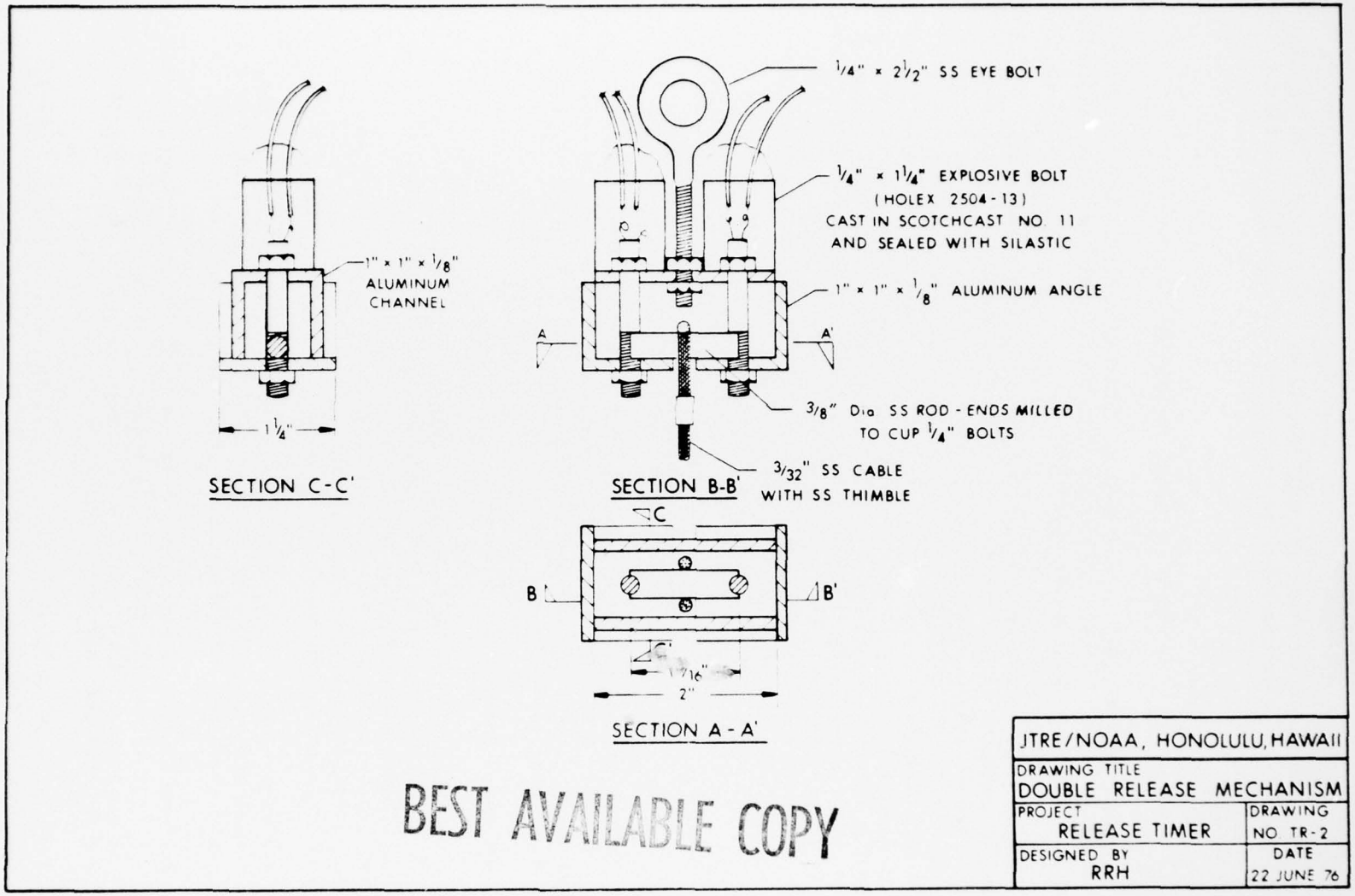


Figure 4. Mechanical drawing of double release mechanism.

capacity since capacity decreases with decreasing temperature. A battery pack of three "D" alkaline cells is sufficient for most applications.

4. DOUBLE RELEASE MECHANISM

The electronic timer is designed to activate various release devices, as described above. We illustrate one such double release device which is used with bottom current meter moorings.

Figure 4 shows the arrangement employing two explosive bolts, either of which separates an anchor from the instrument above. With the exception of the explosive bolts, whose preparation is explained by Byrne and Mitiguy (1977), all parts are either available off-the-shelf or need only minor machining of standard stock. The device is tested to a static load of 400 kg and is used with a working load of 20 kg. Since larger, stronger explosive bolts are available the double release can be rated for greater loads, simply by scaling up the mechanical parts while retaining the identical trigger devices. For long submersion the bolts should be electrically isolated from the aluminum parts; alternatively the aluminum channel and angles could be replaced by stainless steel.

5. RELEASE TIMER TEST SET

The release timer test set is a portable, battery operated, self-contained unit designed to test the integrity of the release by exercising all of its functional parts, individually and together, at an accelerated rate just prior to launching.

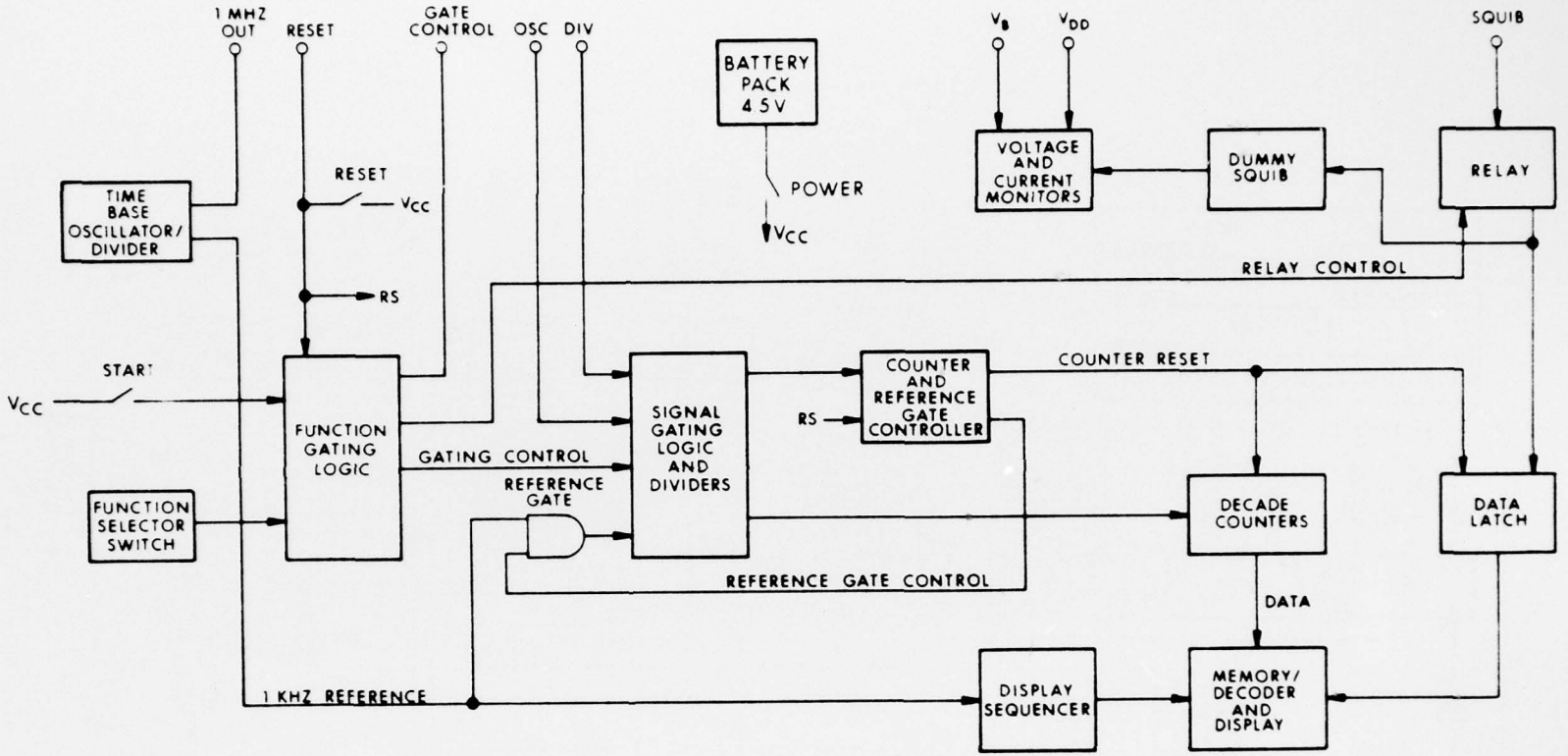
The tests include:

1. measurement of release timer supply current (CUR)
2. measurement of time base oscillator period (OSC)
3. functional test of binary divider chain (DIV)
4. measurement of release timer battery voltages under load
5. verification of programmed time interval (HR)
6. functional test of squib firing circuit

The first test (CUR) in the checkout of the release timer is the measurement of leakage current which indicates the general health of the integrated circuits; subsequent tests (OSC, DIV, HR) are functional.

A block diagram of the test set is shown in Figure 5; circuit details appear in the schematic diagrams (Figs. 6-8). The power source for the test set consists of three alkaline "D" cells connected in series to produce 4.5 V. The test set draws approximately 350 mA.

The time base oscillator generates a 1 MHz signal used for checking the release timer counters and dividers at an accelerated rate. A 1 kHz



JTRE/NOAA HONOLULU, HAWAII	
DRAWING TITLE TEST SET BLOCK DIAGRAM	
PROJECT TEST SET, RELEASE TIMER	DRAWING NO TR4
DESIGNED BY AIN	DATE 1-18-77

Figure 5. Block diagram of release timer test set.

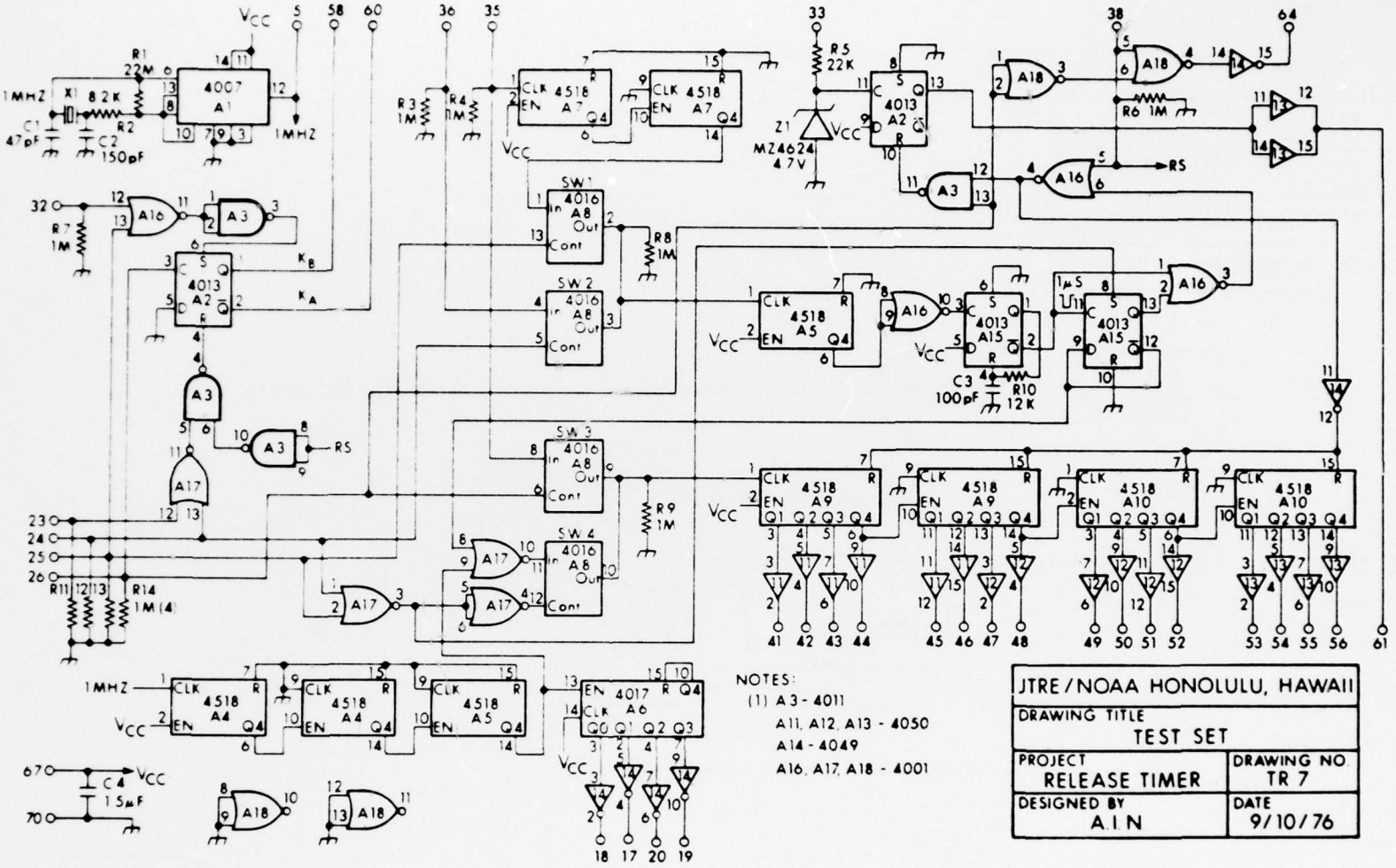
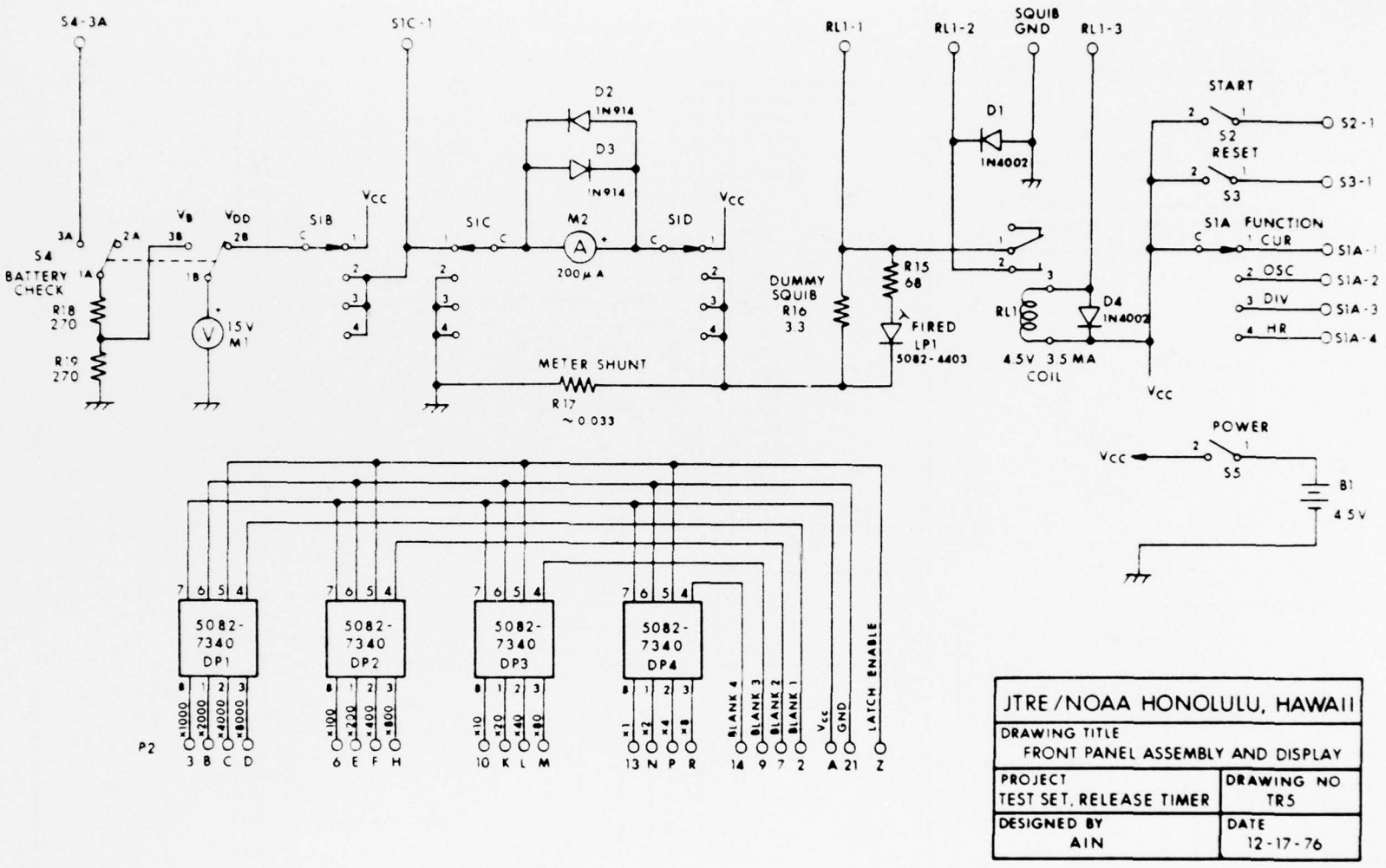


Figure 6. Circuit diagram of release timer test set.



JTRE/NOAA HONOLULU, HAWAII	
DRAWING TITLE FRONT PANEL ASSEMBLY AND DISPLAY	
PROJECT TEST SET, RELEASE TIMER	DRAWING NO TR5
DESIGNED BY AIN	DATE 12-17-76

Figure 7. Circuit diagram of front panel assembly and display for release timer test set.

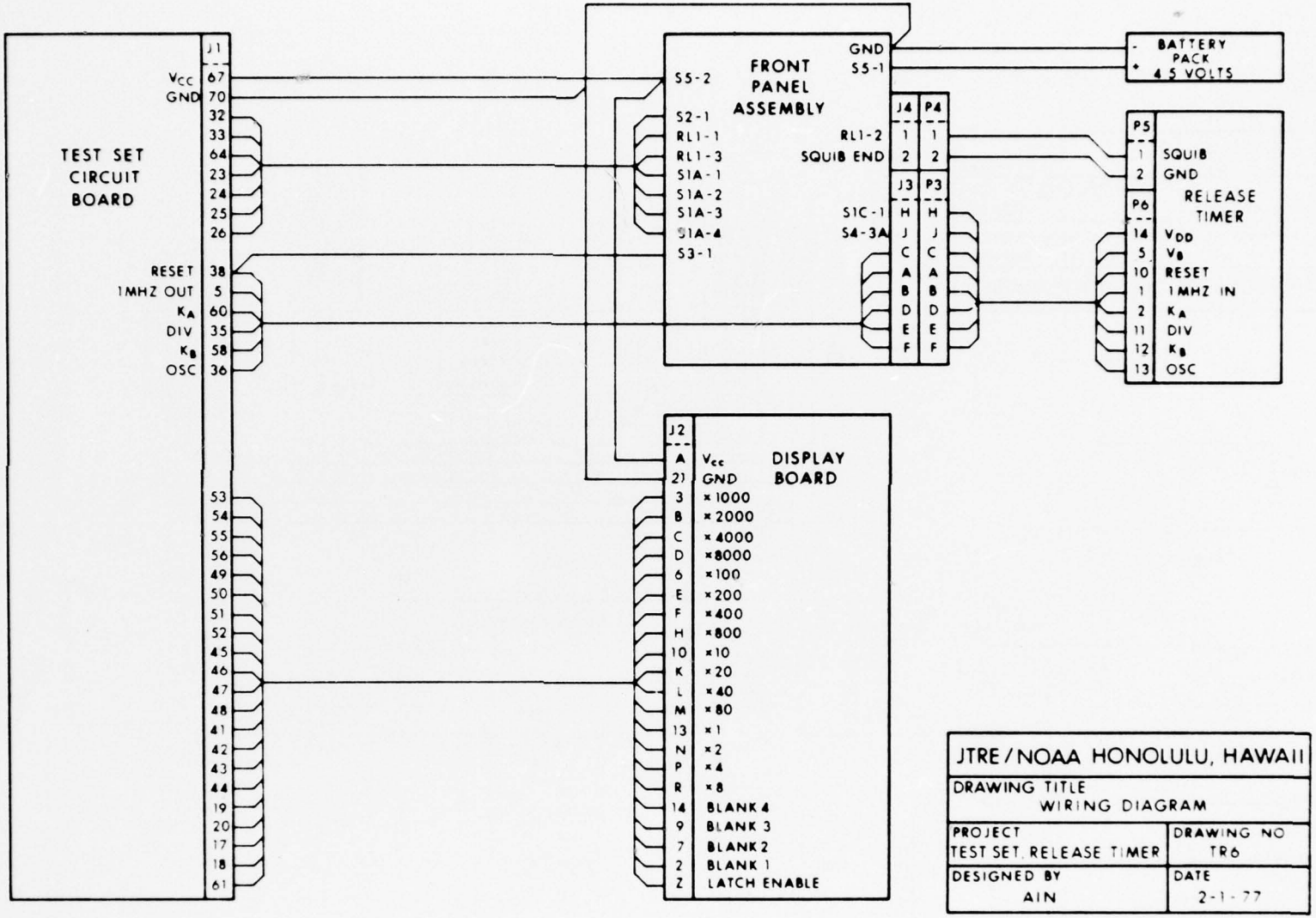


Figure 6. Wiring harness diagram for release timer test set.

reference signal, generated by a divide-by-1000 counter (A4, A5), is used as a time base for making period measurements.

The numerical displays (DP1, DP2, DP3, DP4) used in the test set are Hewlett-Packard[3] type 5082-7340 which contain a decoder, LED drivers, memory, and an input for blanking the display without destroying the contents of the memory. The blanking feature is used for conserving battery power by having only one display on at any given instant. A decade counter, A6, with 10 decoded decimal outputs is used as a display sequencer for driving the blanking inputs. Since there are only four displays, the decade counter is reset to zero by the fifth output (Q4). The counter is driven by the 1 kHz reference signal so that each digit is on for 1 ms out of every 4 ms.

The first test requires the function selector switch in the CUR position and the release timer power switch OFF. Power is supplied to the release timer by the test set and current is monitored by the ammeter. The supply current varies between different units, but should not exceed 100 μA. Excessive current drain implies that one or more integrated circuits are defective and should be replaced. The voltmeter monitors the test set battery voltage which should be at least 4.0 V.

For the CUR test, a high logic level passes through switch S1A to gates A3 and A17, forcing gate control flip-flop A2 (in the test set) to reset, which brings gate control signal K_A and K_B to logical "1" and "0," respectively. In this condition the AND/OR gate A2 (in the timer) routes the output from the first divider, A1, to the second divider, A3, corresponding to the normal operating state of the release timer. Power is supplied to the release timer from the test set V_{CC} supply through switches S1D and S1C, via the ammeter, M2, thence to V_{DD} on the test socket.

During the second test, the function selector switch is in the OSC position and the release timer power switch ON. This test checks the time base oscillator, the first divider, and the AND/OR gate. The numerical display shows the average period of 10 cycles of the output from the first divider; a reading of 8789 indicates that the circuits are functioning properly. In the OSC position the ammeter is disconnected while the voltmeter monitors the release timer battery voltage (which should be at least 4.5 V).

Basically, the OSC measurement is made by counting the 1 kHz reference signal for an integral number of cycles of the signal being measured. The accumulated count displayed thus becomes a measure of the average period of the signal with an effective resolution of 0.1 ms for a 10-cycle count.

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[3]REFERENCE TO TRADE NAMES DOES NOT IMPLY ENDORSEMENT BY THE ENVIRONMENTAL RESEARCH LABORATORIES, NOAA.

Flip-flop A2 in the test set is kept in the reset state as in the CUR test, putting the release timer in its normal operating state. The output from the AND/OR gate in the release feeds through solid state switch SW2 (A8) into the 10-period counter A5 of the test set. The output from A5 goes to the input of A15, the counter and reference gate controller. One-half of A15 is used as a one-shot. The second half is a divide-by-two counter whose output controls the 1 kHz reference gate. This 1 kHz signal is alternately gated on for 10 periods and off for 10 periods of the input to A5.

The counter and reference gate controller, A15, also generates a signal which resets the decade counters A9 and A10 to zero before each counting sequence. The 10-period average of the input to A5 accumulates in A9 and A10 and is passed on to the display buffers A11, A12, and A13, and then to the displays DP1, DP2, DP3, and DP4.

In the third test, the function selector switch is set to the DIV position. Proper operation of the second divider in the timer is checked by feeding an external 1 MHz signal into the divider and measuring the period of the output. A count of 4096 indicates that the second divider is working properly. As in the second test, the voltmeter monitors the release timer battery voltage and the ammeter is disconnected.

Gate control flip-flop, A2, is forced into the set state by switch S1A and gates A3 and A16. K_A is now at logical "0" and K_B at logical "1." This combination causes the AND/OR gate (A2 in the release timer) to connect the test set 1 MHz signal to the input of the second divider, A3. The output from inverter A4 in the release timer goes to the divide-by-100 counter, A7, through the solid state switch SW1, thence to the period measurement circuits described in the OSC test. Note, however, that the display shows a 1000-period average rather than a 10-period average.

The final test verifies the programmed time interval and checks the integrity of the release timer batteries and firing circuit. The function selector switch is set to the HR position. The test sequence is started by first depressing the RESET switch to zero all of the test set counters and then depressing the START switch. The countdown of the programmed time interval on the release timer is accelerated by driving it with the 1 MHz signal from the test set.

When the firing circuit is activated, the numerical display shows the number of hours set on the release timer, which should correspond to the number set on the programming switches. The ammeter monitors the firing current, which is limited to approximately 1 ampere by the dummy squib resistance in the test set. The voltmeter indicates the condition of the release timer batteries under this heavy load. The FIRED lamp lights when the firing current flows. After a few seconds, the RESET switch should be depressed to reset the firing circuit, since this test loads the batteries heavily.

If the high current pulse activator option is used, the FIRED lamp will momentarily light and the ammeter will indicate a pulse of current when the firing circuit is activated. The numerical display shows the programmed time interval. The 24-V battery is checked under a 540 ohm (45 mA) load by switching the Battery Check switch to V_B. The voltmeter indicates half the actual battery voltage.

Switching the function selector to the HR position toggles gate control flip-flop A2 to the reset state, forcing the release timer to its normal operating state.

A logical "1" from switch S1A-4 through gates A18-3 and A18-4 forces the output of A14-15 to a logical "0." Current flowing through relay coil RL1 closes the relay contacts, completing the path from SCR1 in the release timer through the dummy squib resistor R16, ammeter M2, meter shunt R17, and to ground return. SCR1 can now be activated and it will latch "on" if triggered. In the other tests, the relay is not energized and the relay contacts are open, preventing SCR1 from latching in the "on" state.

When the RESET switch in either the test set or the release timer is depressed the following actions take place:

1. The numbers set on the programming switches in the release timer are loaded into the four decade down counters A5, A6, A7, and A8.

2. Decade counters A9 and A10 in the test set are reset to zero and displayed.

3. Data latch A2 is reset.

4. Relay coil RL1 is de-energized, opening the squib current path and enabling SCR1 to turn off if previously activated. The relay is de-energized as long as the RESET switch is depressed.

5. Gate control flip-flop A2 in the test set is reset, causing the AND/OR gate, A2, in the release timer to gate the time base signal from the first divider, A1, to the second divider, A3.

When the START switch is depressed the following actions take place:

1. Gate control flip-flop A2 in the test set is set, gating the test set 1 MHz signal into the second divider, A3, in the release timer.

2. Each pulse from inverter A4-13 in the release timer increments counters A9 and A10 in the test set and decrements counters A5, A6, A7, and A8 in the release timer.

3. The squib firing circuit is activated when the count reaches zero in A5, A6, A7, and A8 in the release timer.

4. The ammeter registers the squib current.

5. The voltage drop across the dummy squib resistor causes the LED to glow and toggles the data latch flip-flop A2 to the set state. This strobes the data from the decade counters A9 and A10 into display memories.

6. The display shows the count accumulated at the moment the squib circuit was activated.

The release timer log sheet (Fig. 9) and release timer parts list (Fig. 10) are included in this report to assist the reader in utilizing this system.

6. ACKNOWLEDGMENTS

Development of this release is one of many joint National Oceanic and Atmospheric Administration-University of Hawaii projects which were initiated by the late Gaylord R. Miller. We wish to thank Grant Blackinton, Ronald Fukuhara, William Ichinose, Hubert Mattes, and Jean Michel for their useful suggestions and assistance. This project was supported by NOAA contract 04-6-022-44015 and Office of Naval Research contract N00014-75-C-0209.

Release Timer Test and Preset Procedure

1. Release timer and test set power off.
2. Connect test set cables to release timer. Match notches on test plug and test socket, squib cables are size coded.
3. Switch to "CUR".
4. Test set power on -- record supply current.
5. Release timer power on.
6. Switch to "OSC" -- record period after second counting cycle.
7. Switch to "DIV" -- record period after second counting cycle.
8. Switch to "HR".
9. Depress release timer "RESET".
10. Depress "START" on test set -- upon firing, record current and count, then reset immediately (firing mode draws 1 amp from batteries).
11. Remove cables from release timer.
12. Depress release timer "RESET" and record reset time.
13. Check and grease O-rings in end caps.
14. Assemble release timer into pressure housing, purging with dry nitrogen or argon, and screw caps hand tight.
15. Connect to release mechanism.

Retrieval and Storage Procedure

1. Disconnect cables and put unfired explosive elements in a safe place.
2. Thoroughly wash release in fresh water.
3. Allow release to come to ambient temperature before opening in a dry place.
4. For storage, purge with dry nitrogen or argon and assemble.

Release Timer Log Sheet

Operator _____

Release # (on endcap) _____

PC board # (on test socket) _____

Preset hours _____

Supply current _____ (< 100 μ a)

Oscillator period _____ (8789)

Divider _____ (4096)

Count at fire time _____ (same as preset hours)

Fire current _____

Date, time (GMT) of RESET _____

Calculated date, time (GMT) of firing _____

Comments _____

Figure 5. Instructions for testing release timer and sample log sheet.

[A]

Integrated Circuits--All IC's are CMOS in ceramic dual-in-line packages.
A1 - 4060
A2 - 4019
A3 - 4040
A4 - 4002
A5, A6, A7, A8 - 4510

Transistors
Q1, Q2 - 2N2222A

Silicon Controlled Rectifier
SCR1 - 2N4184

Resistors--All resistors are ¼ watt, 5% tolerance.
R1, R2, R5, R6, R7, R8, R12 - 100K
R3 - 22M
R9 - 27K
R10 - 27
R11 - 470
R13 - 22K

Capacitors
C1 - 50 pF
C5, C6 - 0.68 µF 35 WVDC tantalum
C7 - 150 pF
C8, C9 - 750 µF 25 WVDC tantalum

Quartz Crystal
X1 - Statek Corp. type SX-1H, 18641 Hz

Switches
S1 - DPST miniature toggle
S2 - SPDT momentary contact miniature toggle
S3, S4, S5, S6 - SPDT rocket DIP switch Grayhill Inc. type 76C04

Miscellaneous
Test socket - 14 pin DIP IC socket
Waterproof connector (2 contact 20,000 psi) Vector part number XSG2BCL

[B]

Integrated Circuits--All IC's are CMOS in ceramic dual-in-line packages.
A1 - 4007
A2, A15 - 4013
A3 - 4011
A4, A5, A7, A9, A10 - 4518
A6 - 4017
A8 - 4016
A11, A12, A13 - 4050
A14 - 4049
A16, A17, A18 - 4001

Display
DP1, DP2, DP3, DP4 - Hewlett-Packard type 5082-7340

Resistors - All resistors are ¼ watt, 5% tolerance unless noted otherwise.
R1 - 22M
R2 - 8.2K
R3, R4, R6, R7, R8, R9, R11, R12, R13, R14 - 1M
R5 - 22K
R10 - 12K
R15 - 68 ½ watt
R16 - 3.3 8 watt
R17 - approximately 33 milliohms 20 AWG hookup wire wound on 1MΩ 2W resistor used as coil form. Calibrate meter by cut-and-try method.
R18, R19 - 270 1 watt

Capacitors
C1 - 47 pF
C2 - 150 pF
C3 - 100 pF
C4 - 1.5 µF 20WVDC

Quartz Crystal
X1 - 1.000000 MHz

Zener Diode
Z1 - MZ4624 4.7 volts

Diodes
D1, D4 - 1N4002
D2, D3 - 1N914

LED
LP1 - Hewlett-Packard 5082-4403

Relay
RL1 - SPDT 4.5 volt 3.5 mA coil

Switches
S1 - 4-pole 4-position rotary
S2, S3 - SPST normally open push button
S4 - DPDT momentary contact miniature toggle
S5 - SPST miniature toggle

Meters
M1 - voltmeter 0-15 V
M2 - ammeter 0-200 µA

Figure 10. Release timer parts list (A) and release timer test set parts list (B).

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